

REMARKS

Applicant respectfully thanks the Examiner for acknowledging both the claim for foreign priority in this Application as well as the previously filed Information Disclosure Statement.

Applicant respectfully notes that the Office Action contains a minor typographical error on page 2, paragraph 1, in that the present application was filed on 8/15/2006 (vice 8/25/2006).

In response to the Office Action mailed July 2, 2008, Applicant requests reconsideration based on the amendments herein and at least the following remarks. Applicant respectfully submits that the claims as presented herein are in condition for allowance.

Claims 1-39 are pending in the present application. Claims 1, 11 and 26 have been amended.

No new matter has been added by the amendments. Specifically, support for the amendments to claim 1 can be found at least at FIG. 1 and page 13, second full paragraph (corresponds to paragraph [0044] of the published application) of the application as filed. Support for the amendments to claims 11 and 26 can be found at least in FIGS. 3, 4 8, 9A and 9B, as well as at page 17, second and third full paragraphs (corresponds to paragraphs [0064] and [0065] of the published application).

Applicant respectfully requests reconsideration of claims 1-39 based upon the amendments and at least the following remarks.

Title

The Title stands objected to, on page 2 of the Office Action, for not being descriptive. It is respectfully noted that the Title has been amended to more fully describe an exemplary embodiment of the present invention, i.e., that the method is directed toward a data communication method for the chip design verification apparatus, as indicated by the amendment to the Title above. No new matter has been

added. Therefore, it is respectfully requested that the objection to the Title be withdrawn.

Abstract

The Abstract stands objected to for exceeding 150 words and for including legal phraseology such as the words “means” and “said” therein. It is respectfully noted that the Abstract has been amended to correct the abovementioned deficiencies, as well as to correct minor grammatical and antecedent basis errors, as indicated by the amendments to the Abstract of the Disclosure above. No new matter has been added. Therefore, it is respectfully requested that the objection to the Abstract be withdrawn.

Specification

The disclosure is objected to for informalities, i.e., numerous grammatical errors, such as in paragraphs [0050], [0099], [0101] and [0189], as described on pages 2 and 3 of the Office Action. It is respectfully noted that the specification has been amended to correct the abovementioned grammatical errors, as well as additional grammatical and antecedent basis errors, as reflected in the substitute specification (both clean and marked-up versions are attached hereto). Therefore, it is respectfully requested that the objection to the Specification be withdrawn.

Claim Objections

Claim 1 stands objected to for informalities. Specifically, the Examiner states that the word “and” should be deleted from line two of claim 1. It is respectfully noted that claim 1 has been amended, *inter alia*, to comply with the Examiner’s suggestion. Therefore, it is respectfully requested that the objection to claim 1 be withdrawn.

Claim Rejections Under 35 U.S.C. §112

Claims 1, 11 and 26 stand rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential cooperative relationships of elements, i.e., where the hardware block and the software block are arranged. Claims 2-10, 12-25 and 27-39 stand rejected as depending from claim 1, 11 and 26.

It is respectfully noted that claims 1, 11 and 26 have been amended to more clearly disclose the arrangement of the hardware block and the software block. Specifically, the abovementioned claims have been amended to disclose that the hardware block is included in the target unit, while the software block is included in the computer.

Accordingly, it is respectfully requested that the above rejection to claims 1-39 under 35 U.S.C. § 112, second paragraph, be withdrawn.

Claim Rejections Under 35 U.S.C. §101

Claims 11 and 26 stand rejected under 35 U.S.C. § 101 as being allegedly directed to non-statutory subject matter, as stated on pages 3-4 of the Office Action. Specifically, the Examiner states that that, while claims 11 and 26 are useful and concrete, there does not appear to be a tangible result claimed. Claims 12-25 and 27-39 stand rejected as depending from claims 11 and 26. Applicant respectfully traverses for at least the following reasons.

Applicant respectfully submits that the subject matter of claims 11 and 26 does not fall under a judicial exception as delineated in MPEP 2106. Specifically, the invention disclosed in claims 11 and 26 is not a “law of nature”, “natural phenomena” or “abstract idea”. Instead, the present invention of claims 11 and 26, as amended, is directed toward a data communication method including, *inter alia*, steps of transmitting data, determining the validity of the data, and then, based on the determination, further applying (e.g., transmitting/receiving) valid data. Therefore, the subject matter of claims 11 and 26 is clearly directed toward a process, and thus the requirements discussed in MPEP 2106.IV.C.2 (pertaining to

transformation/useful, concrete and tangible results associated with judicial exceptions) do not apply to the present invention.

Accordingly, it is respectfully requested that the above rejection to claims 11-39 under 35 U.S.C. § 101 be withdrawn.

Claim Rejections Under 35 U.S.C. §102

To anticipate a claim under 35 U.S.C. § 102, a single source must contain all of the elements of the claim. *Lewmar Marine Inc. v. Barient, Inc.*, 827 F.2d 744, 747, 3 U.S.P.Q.2d 1766, 1768 (Fed. Cir. 1987), cert. denied, 484 U.S. 1007 (1988). Furthermore, the single source must disclose all of the claimed elements “***arranged as in the claim.***” *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716, 223 U.S.P.Q. 1264, 1271 (Fed. Cir. 1984) (Emphasis added).

Claim 1-39 stand rejected under 35 U.S.C. § 102(e) as being allegedly unpatentable over Park et al. (U.S. Patent No. 7,185,295, hereinafter “Park”) as stated on pages 4-12 of the Office Action. The Examiner states that Park discloses all of the elements of the abovementioned claims, primarily at X. Applicant respectfully traverses for at least the following reasons.

Applicant respectfully notes that Park teaches, primarily at FIGS. 2 and 14a and column 17, lines 49-56, a chip design testing apparatus and method, wherein when a CPU compares input data with expected data and determines whether the input data is consistent with expected data; if not, the CPU attempts to determine a location of a mismatch, i.e., re-determines a comparison starting location. If, on the other hand, the input data is consistent, this indicates that a last frame has been received (correctly) and processing stops (see, e.g., FIG. 14a and col. 17, lines 53-54).

In contrast and in accordance with the present invention, as disclosed in independent claim 1, and similarly in claims 11 and 25, discussed below, however, the interface means actually applies **only** the valid output data of the software block

to the hardware block (and/or the valid output data of the hardware block to the software block) after determining the validity thereof.

In addition, the CPU corresponds to the controller of claim 1 in the present invention. Thus, the interface of Park does not discriminate or output only valid data, as does the interface of the present invention.

Thus Park does not teach or suggest “an **interface means** of transmitting output data of the hardware block, determining whether output data of the software block is valid, and **applying only valid output data of the software block to the hardware block**...and a controller for transmitting the output data of the software block generated by an operation of executing the chip design verification program to the interface means, determining whether the output data of the at least one hardware block input via the interface means is valid, and **applying only valid output data of the at least one hardware block to the at least one software block**”, as in amended independent claim 1. Therefore, Park does not disclose all of the claimed elements arranged as in amended claim 1.

Accordingly, it is respectfully submitted that claim 1, including claims depending therefrom, i.e., claims 2-10, define over Park.

In addition regarding dependent claims 3 and 4, the disclosure of Park at column 17, lines 59-62 and col. 18, lines 12-21, pointed out by the Examiner at page 8 of the Office Action, relate to the functions of trigger condition controller (64 in FIG. 5 of Park), and thus correspond to the trigger condition controller (564) in FIG. 5 of the present invention. Thus, Clark does not teach or suggest the functions of the chip design verification program as disclosed in the instant application and claimed in claims 3 and 4 thereof.

Furthermore, the interface means of the present invention generates multi clocks, but Park merely teaches “... inputting the clock signals [i.e., signals from a given, single, clock] applied to the target ...” (see, e.g., column 18, lines 12-21).

Thus, Park fails to teach or suggest “a multi clock setting value for operating the software block and the hardware block” (claim 3) or “generating multi clocks in response to the multi clock setting value” (claim 4).

Accordingly, it is respectfully submitted that claims 3 and 4, including claims depending therefrom, i.e., claims 5-10, define over Park for these additional reasons, as well.

Additionally and with regard to dependent claims 5 and 8, Park is silent as to any system clock count value. Therefore, Park fails to teach or suggest “wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed” (claim 5) or “wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed” (claim 8).

Accordingly, it is respectfully submitted that claims 5 and 8, including claims depending therefrom, i.e., claims 6, 9 and 10, define over Park for these additional reasons, as well.

Regarding independent claims 11 and 26, it is respectfully noted that, as described above with reference to independent claim 1, Clark fails to teach or suggest applying only valid output data to the hardware and software blocks.

Thus Park does not teach or suggest “applying only the valid output data of the hardware block to the software block...and applying only the valid output data of the software block to the hardware block”, as in amended independent claims 11 and 26. Therefore, Park does not disclose all of the claimed elements arranged as in amended claims 11 and 26.

Accordingly, it is respectfully submitted that claims 11 and 26, including claims depending therefrom, i.e., claims 12-25 and claims 27-39, respectively, define over Park.

In addition regarding dependent claim 12, the interface means of the present invention generates multi clocks, which is lacking in Park, as described above.

Thus, Park fails to teach or suggest “a step of allowing the chip design verification program to obtain a multi clock setting value to be provided to the interface means, and generate multi clocks in response to a system clock of the chip design verification program and the multi clock setting value to be applied to the software block; and a step of allowing the interface means to generate multi clocks in response to the system clock of the interface means and the multi clock setting value to be applied to the hardware block” as in claim 12.

Accordingly, it is respectfully submitted that claim 12, including claims depending therefrom, i.e., claims 13-25, define over Park for these additional reasons, as well.

Furthermore regarding dependent claims 13, 15, 27, and 29, Park is silent as to any system clock count value. Therefore, Park fails to teach or suggest “wherein the output data of the hardware block has an output value of the hardware block changed in response to the multi clocks applied from the interface means, and a system clock count value of the interface means when the output value of the hardware block is changed” (claim 13 and 27) or “wherein output data of the software block has an output value of the software block changed in response to the multi clocks applied from the chip design verification program, and a system clock count value of the chip design verification program when the output value of the software block is changed” (claims 15 and 29).

Accordingly, it is respectfully submitted that claims 13, 15, 27 and 29, including claims depending therefrom, i.e., claims 14-21, 23-25, 28 and 30-39 define over Park for these additional reasons, as well.

Therefore, for at least the abovementioned reasons, it is respectfully requested that the above rejections to claims 1-39 under 35 U.S.C. § 102(e) be withdrawn.

Claims 1, 11, and 26 stand rejected under 35 U.S.C. § 102(e) as being allegedly anticipated by Schubert et al. (U.S. Patent No. 7,240,303, hereinafter “Schubert”). The Examiner states that Schubert discloses all of the elements of the abovementioned claims, primarily at FIGS. 20, 21 and 33B, as well as at columns 13 and 53-59. Applicant respectfully traverses for at least the reasons set forth below.

Applicant respectfully notes that Schubert teaches a hardware and software debugging system wherein when certain trigger conditions, a debugger is notified and thereafter system operations are halted and/or a snapshot of the system is taken for later analysis (see, e.g., column 57 line 27 through column 58 line 17 of Schubert). Schubert is completely silent, however, as to any teaching or suggestion that

In contrast and in accordance with the present invention, as disclosed in independent claims 1, 11 and 26, the interface means discriminates to determine the valid output data of the software block and applies only the valid data to the hardware block, as described in greater detail above with reference to Park.

Thus Schubert does not teach or suggest “a **controller** for transmitting the output data of the software block generated by an operation of executing the chip design verification program to the interface means, **determining whether the output data of the at least one hardware block input via the interface means is valid**, and applying **only** valid output data of the at least one hardware block to the at least one software block”, as in amended independent claim 1. Likewise, Schubert fails to teach or suggest “a software side operation step of transmitting output data generated by the operation of the software block to the interface means, **determining whether the output data of the hardware block received via the interface means is valid** by executing the chip design verification program, and applying **only** the valid output data of the hardware block to the software block; and a hardware side operation step

of transmitting output data generated by the operation of the hardware block to the software block, **determining whether the output data of the software block received is valid** by executing the chip design verification program in the interface means, and applying **only** the valid output data of the software block to the hardware block”, as in amended independent claims 11 and 26.

Therefore, Schubert does not disclose all of the claimed elements arranged as in amended claims 1, 11 and 26.

Accordingly, it is respectfully submitted that claims 1, 11 and 26, including claims depending therefrom, i.e., claims 2-10, 12-25 and 27-39 define over Schubert.

Therefore, it is respectfully requested that the above rejection to claims 1, 11 and 26 under 35 U.S.C. § 102(e) be withdrawn.

Conclusion

In view of the foregoing remarks distinguishing the prior art of record, Applicant respectfully submits that this application is in condition for allowance. Early notification to this effect is requested. The Examiner is invited to contact Applicant's attorneys at the below-listed telephone number regarding this Amendment or otherwise regarding the present application in order to address any questions or remaining issues concerning the same. If there are any charges due in connection with this response, please charge them to Deposit Account 06-1130.

Respectfully submitted,

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